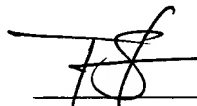




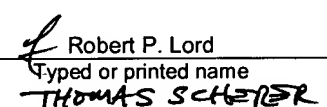
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PRE-APPEAL BRIEF REQUEST FOR REVIEW		Docket Number (Optional) 16159/089001; P4777	
		Application Number 09/990,935-Conf. #2886	Filed November 15, 2001
		First Named Inventor William K. Lam	
		Art Unit 2123	Examiner T. H. Stevens
<p>Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.</p> <p>This request is being filed with a notice of appeal.</p> <p>The review is requested for the reason(s) stated on the attached sheet(s). Note: No more than five (5) pages may be provided.</p> <p>I am the</p> <p><input type="checkbox"/> applicant /inventor.</p> <p><input type="checkbox"/> assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)</p> <p><input checked="" type="checkbox"/> attorney or agent of record. Registration number <u>46,479</u></p> <p><input type="checkbox"/> attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34. _____</p> <p>NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.</p>			

 #45,079

Signature



Typed or printed name
THOMAS SCHERER

(713) 228-8600
Telephone number

January 30, 2006
Date

☐ *Total of 1 forms are submitted.

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the U.S. Postal Service as Express Mail, Airbill No. EV766455885US, on the date shown below in an envelope addressed to:
MS AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Dated: January 30, 2006

Signature  (Brenda C. McFadden)



I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the U.S. Postal Service as Express Mail, Airbill No. EV766455885US, on the date shown below in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Dated: January 30, 2006

Signature

Brenda C. McFadden
(Brenda C. McFadden)

Docket No.: 16159/089001; P4777

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
William K. Lam

Conf. No.: 2886

Application No.: 09/990,935

Art Unit: 2123

Filed: November 15, 2001

Examiner: T. H. Stevens

For: METHOD AND APPARATUS FOR
AMORTIZING CRITICAL PATH
COMPUTATIONS

MS AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRE-APPEAL BRIEF REQUEST FOR REVIEW

In response to the Advisory Action dated December 28, 2005, Applicant responds with this pre-appeal brief request for review.

Claims 1, 3-6, 8-11, 13-16, 18-21, 23-26, and 28-30 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,095,454 issued to Huang (hereinafter "Huang"), in view of U.S. Patent No. 6,339,837 issued to Li (hereinafter "Li"), and in further view of U.S. Patent No. 6,637,014 issued to Casavant (hereinafter "Casavant"). In maintaining the above rejection and issuing a final Office Action, Applicant respectfully asserts that the Examiner has failed to satisfy the requirements set out in MPEP §§ 2141.01(a) and 2143.

As a first matter, Applicant asserts the Casavant reference is non-analogous art. During the simulation of a digital circuit design, the digital circuit design is represented by a data flow graph with one or more path(s) traversing the data flow graph. These paths may have different lengths representing different computational times. The claims of the present invention are focused towards reducing the difference between the longest ("critical") and shortest paths thereby reducing the overall simulation time of the digital circuit design. In contrast, Casavant is focused on mitigating crosstalk in an integrated circuit. Crosstalk is

interference caused by electric power being coupled from one circuit into adjacent circuits. Accordingly, mitigating crosstalk is not related to reducing the execution time of a cycle-based simulation, nor is it even related to cycle-based simulations in general. Thus, as Casavant is neither in the field of applicant's endeavor nor reasonably pertinent to the particular problem with which Applicant is concerned, Casavant is non-analogous art because it fails to meet the requirements of MPEP §2141.01(a).

As a second matter, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. (See MPEP §2143).

Huang discloses a method and apparatus for verifying timing during simulation of digital circuits. Further, one objective of Huang's method and apparatus is to provide two paths through the circuitry which are the minimum ("shortest") and maximum ("critical") paths from input node to output node. (See, e.g., Huang at column 2, lines 28-37 and column 5, lines 45-55). Similarly, Li discloses a method for verifying a digital circuit design in a hardware description language using a verification structure and a verification engine. (See Li at Abstract). In contrast, Casavant is focused on mitigating crosstalk in an integrated circuit. As discussed above, Crosstalk is interference caused by electric power being coupled from one circuit into adjacent circuits.

Even assuming *arguendo* that Li and Huang are properly combinable, Applicant asserts there is no motivation to combine the teachings of Huang and Li with the teachings of Casavant. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must *both* be found in the prior art, *not* in Applicant's disclosure. *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991) (emphasis added). Further, the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680 (Fed. Cir. 1990). In other words, there must be some objective reason to combine the teachings of the reasons. *Ex parte Levengood*, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993).

A complete study of Casavant, Li, and Huang confirms that, regardless of whether the teachings of Casavant, Li, and Huang *can* be combined, there is no suggestion or motivation set forth in Casavant, Li, or Hung to combine the teachings of these references. Absent such a suggestion or motivation, the teachings of Casavant, Li, and Huang cannot be conveniently combined to render the claimed invention obvious.

In view of the above, Applicant respectfully asserts the Examiner has failed to establish a *prima facie* case of obviousness because any motivation to combine Casavant, Li, and Huang is unrealistic and improper. Accordingly, claims 1, 3-6, 8-11, 13-16, 18-21, 23-26, and 28-30 are patentable over Casavant, Li, and Huang.

Further, Applicant asserts the prior art references, whether considered separately or in combination, do not teach or suggest all the claim limitations. Specifically, independent claim 1 recites, in part, “wherein simulation further comprises reducing a difference between said critical path and a shortest path in said data flow graph.” Independent claims 11 and 21 have similar limitations. The Examiner has attempted to equate this limitation with modifying timing graph paths as disclosed in Casavant. (See Final Office Action dated October 13, 2005). This association is improper as the paths disclosed by Casavant relate to crosstalk within an integrated circuit and thus are not the same as the paths disclosed in the instant specification and recited in the claims.

During a cycle-based simulation, a digital circuit design is represented by a data flow graph with one or more path(s) traversing the data flow graph. The lengths of the paths are related to the execution time of the cycle-based simulation. It would be clear to one skilled in the art that the lengths of all paths, especially the longest (“critical”) path, should be minimized to reduce the overall time required to execute the cycle-based simulation. (See, e.g., Instant Specification at page 7, line 11 to page 8, line 11). As Casavant actually contemplates increasing the lengths of the timing graph paths (see Casavant at column 15, lines 44-66), it is clear the timing graph paths in Casavant are not the same as the paths recited in the claims. Thus, Casavant does not teach each and every limitation of independent claims 1, 11, and 21.

As discussed above, Huang discloses a method and apparatus for verifying timing during simulation of digital circuits. Further, one objective of Huang’s method and apparatus

is to provide two paths through the circuitry which are the minimum (“shortest”) and maximum (“critical”) paths from input node to output node. However, Huang, like Casavant, is silent on at least reducing the difference between the critical path and the shortest path as recited in amended independent claims 1, 11, and 21. The Examiner has attempted to equate what is disclosed in Huang with the limitations of independent claim 1. (See Office Action dated March 22, 2005). However, Huang discloses finding the shortest and critical paths to check for timing violations (See, e.g., Huang at column 5, lines 45-55), not to reduce a difference between paths as recited in the claims. Thus, Huang does not teach or suggest what Casavant lacks. Thus, Huang does not teach or suggest all limitations of independent claims 1, 11, and 21.

As discussed above, Li discloses a method for verifying a digital circuit design in a hardware description language using a verification structure and a verification engine. Li, like Huang and Casavant, does not teach or suggest reducing the difference between the critical path and the shortest path as recited in independent claims 1, 11, and 21. In fact, Li is solely focused on verifying the functional correctness of the design. (See Li at column 2, lines 39-53). Li is totally silent regarding the critical path, the shortest path, and reducing the difference between them as recited in the claims. Thus, Li does not teach what Casavant and Huang lack. Thus, Li does not teach or suggest all limitations of amended independent claims 1, 11, 21.

In view of the above, the Examiner has failed to show that the prior art references, whether viewed separately or in combination, teach or suggest each and every limitation of independent claims 1, 11, and 21. Thus, the Examiner has failed to satisfy the requirements set forth in MPEP §2143. Accordingly, claims 1, 3-6, 8-11, 13-16, 18-21, 23-26, and 28-30 are patentable over Casavant, Li, and Huang.

Claims 7, 17, and 27 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Huang, in view of U.S. Patent No. 6,856,950 issued to Abts (hereinafter “Abts”), and in further view of Li and Casavant. In maintaining the above rejection and issuing a final Office Action, Applicant respectfully asserts that the Examiner has failed to satisfy the requirements set out in MPEP §2143.

Claims 7, 17, and 27 depend from claims 1, 11, and 21. As discussed above, claims 1, 11, and 21 are patentable over Li, Huang, and Casavant. Abts discloses a system and

method of verifying an electronic system expressed as a logic design. Tests to be run against the logic design are placed within a diagnostic program, and the results of the test are captured and validated against expected results. (See Abts at Abstract). However, like Li, Casavant, and Huang, Abts does not teach or suggest all the limitations of amended independent claims 1, 11, and 21. Abts, like Li, Casavant, and Huang, is silent regarding critical path, shortest path and reducing the difference between them as recited in the claims. Abts is focused on verifying the functional correctness of a logic design, and focuses on abstraction to mask the complexity and implementation details during the verification phase. Thus, Abts is clearly not directed towards amortizing critical path computations as recited in the claims. Further, Abts neither teaches what Casavant, Li, and Huang lack, nor cures the lack of motivation to combine Casavant, Li, and Huang. Thus, independent claims 1, 11, and 21 are patentable over Abts, Casavant, Li, and Huang.

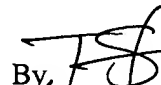
In view of the above, the Examiner has failed to show that the prior art references, whether viewed separately or in combination, teach or suggest each and every limitation of independent claims 1, 11, and 21. Thus, the Examiner has failed to satisfy the requirements set forth in MPEP §2143. Accordingly, claims 1, 3-11, 13-21, and 23-30 are patentable over Abts, Casavant, Li, and Huang.

Conclusion

In view of the above, the Examiner has failed to satisfy the requirements set out in MPEP §2141.01(a) and MPEP §2143. Accordingly, a favorable decision from the panel is respectfully requested. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 16159/089001).

Dated: January 30, 2006

Respectfully submitted,

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